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BINARY CAM WITH CSC TO REINSTATE ATM SWITCH IN ASYNCHRONUS TRANSFER MODE

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ABSTRACT

For packet forwarding and packet classification in networks such as Internet high speed routers are necessary. Now-a-days CAMs are used for this purpose. The Content Addressable Memory (CAM) is a search engine that uses the content of the word to search in the memory. The CAM use up more power during every search operation. Hence, it is vital to reduce power consumption in CAMs. search buss and match buss in CAMs are the major sources of power consumption. Hence, in my project current control blocks are added to each match buss to reduce power consumption. Also parity bits are used find the matched word and reduce the comparison with the miss-matched word. By this way the total power consumption in CAM is reduced to 0.009watts when compared with already existing schemes. CAMs can be used in Asynchronous Transfer Mode (ATM) switching network components as a translation table. CAM can act as an address translator in an ATM switch and perform the VPI/VCI translation very quickly. During the translation process, the CAM takes incoming VPI/VCI values in ATM cell headers and generates addresses that access data in an external RAM.

Keywords : CAM, Current Saving Control, Parity bit, Match bus, Search bus, Tanner.

1 INTRODUCTION

Content-addressable memories (CAMs) are content seek engines that are used for high speed search operations. In conventional memories the search operation is done based on the address of the stored data. Whereas, in CAM the search operation is based on the content of the stored data. CAMs are composed of SRAM for storage and a comparison circuitry which is an XOR gate that enable a search operation to complete in per clock cycle. CAM compares input search data against a table of stored data, and returns the address of the matching data.

For a CAM cell, there are three main parts [7]:

- SRAM Array: The SRAM consists of the path in which the matched location needs to be forwarded.
- Match Bus (MB): For the conventional CAM design, the ML is precharged, and then evaluated to discharge or stay high based on the match or not match decision of the evaluation circuit. The area, power and delay considerations of the ML routing, limits the CAM array size and performance for many applications
- Search Bus (SB): Conventional CAM design uses complementary search lines, which results in a SL activity factor of 1. This high activity factor minimizes the CAM power and delay.

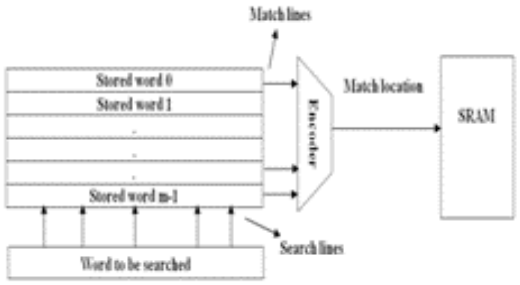


Fig.1. Conventional CAM Cell

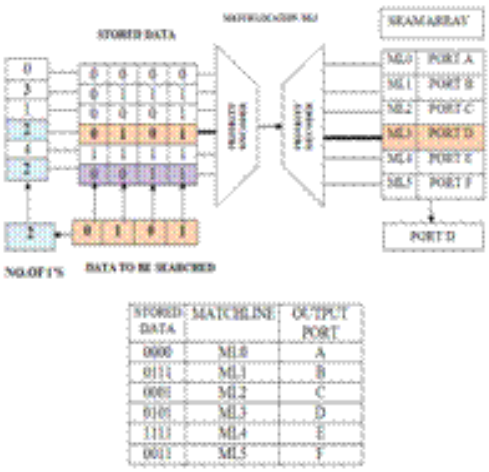
2 STUDY AREA DESCRIPTION

2.1Parity Based CAM

A parity-bit is introduced to boost the search speed of the parallel CAM. A current saving block is used to improve the performance of the CAM comparison in terms of power and robustness. Current saving control block (CSC) is added to each match bus to reduce match bus power consumption. Delay for each search operation is reduced by using parity bits to avoid many miss-match conditions. The overall power consumption is reduced to 0.009 watt for single search.

There are two basic forms of CAM: Binary and Ternary.

2.2 Binary CAM



STORED DATA	MATCHLINE	OUTPUT PORT
0000	ML0	A
0111	ML1	B
0001	ML2	C
0101	ML3	D
1111	ML4	E
0011	ML5	F

Fig.2. Binary CAM Cell

Binary CAMs support storage and searching of binary bits. A basic CAM cell has two basic functions: bit storage as in RAM and bit comparison which is unique to CAM. Data to be searched will be broadcast on to the search lines. The number of 1's from the data to be searched is extracted and is used for comparison with the stored data. Once a match is found the particular match bus will be selected by the parity encoder and it will be matched with the output port accordingly to the table. At the circuit level CAM structure implemented as NAND-type. But at architectural level bit storage uses simple SRAM cell and comparison function is equivalent to XOR operation. The number of bits in a CAM word is usually large, with existing implementations ranging from 36 to 144 bits [3]. A typical CAM employs a table size ranging between a few hundred entries to 32K entries, corresponding to an address space ranging from 7 bits to 15 bits.

2.3 Types of CAM cell

NAND-type CAM cells consists of number cells connected in series to create a long pass transistor network. In case of a match, a signal driven from one end of the ML propagates to the other end [4]. In case of a mismatch, the signal is stopped by the first mismatched CAM cell, as it turns off its corresponding pass transistor. Since on average most MLs are mismatched, the signal is stopped within the first two pass transistors, reducing the switching activity of the ML and saving power.

Drawback

- The NAND ML architecture suffers from long search delays.

NOR ML architecture is preferred for higher speed. The NOR architecture consists of CAM cells that are connected in parallel, instead of in series. When the search data is applied to the SLs, the bit-compare circuit in each CAM cell compares each search bit to its corresponding stored bit. A CAM cell storing a matching bit will isolate the ML from GND, while the one with a mismatched bit creates a path to GND through its bit-compare circuit. If all the bits in a stored word are identical to those of the search word, the ML has no path to GND, and remains in the high-impedance state. On the other hand, if there is one or more bit mismatches, one or more paths to GND are created, and the ML impedance is reduced accordingly[4].

2.4 Ternary CAM

A binary CAM stores and searches only "0"s and "1"s. However, binary cannot satisfy the fast commercial application, and the utility of CAM is limited. A ternary CAM (TCAM) can perform partial matching. The TCAM has an ability to find the longest prefix matching for comparing a search data with its cell contents to find all matching prefixes and determine the longest prefix in one clock cycle. This feature can used in high speed Internet routers because these applications need to find the longest matching prefix in growing lookup tables. A content cell in TCAM can be in one of three states: don't care (X) and binary states (0, 1). The "X" is a don't care condition, that represents both "0" and "1", allowing an unpredictable operation. Unpredictable operation means that an "X" value stored in a cell causes a match regardless of the input bit [4].

2.5 Parity bit generator

In conventional CAM the count of 1's in the search word is taken into account. As the count increases the memory required is also increased. To overcome the issue parity bit is used to reduce the miss-match condition. For search word with even number of 1's 0 will be its parity bit value and for odd number of 1's 1 will be its parity bit value. The parameter extractor will be used to find this value. By this way the search speed is increased and also the storage space required is reduced. The parity bit generator can bit used for this purpose.

2.6 Software setup

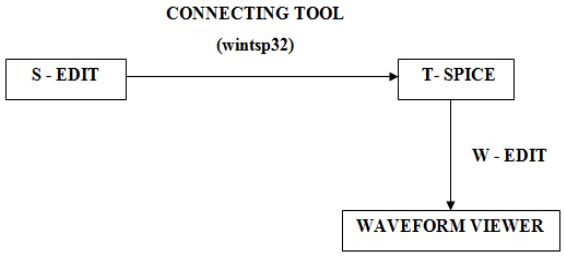


Fig.3. Tanner software setup

S- Edit saves and reads design files in Tanner Research's proprietary S- Edit Database (SDB) format. An SDB file contains design information and setup information. S- Edit has two viewing modes: schematic mode and symbol mode. By using wintsp32 application T-Spice tool can be used to insert commands and files. Commands for adding voltage sources, transient analysis, input bit-stream and output constant can be done by using INSERT COMMAND tab.Once the program has been simulated without error, W-Editor can be used to analyze the waveform of given input and its corresponding output

3 SYSTEM IMPLEMENTATION

3.1 Existing methods

3.1.1 Selective pre-charge and pipe-line architecture
In selective precharge method, mixed NAND/NOR match bus structure is used. The match bus is divided into segments. The ML is precharged through the transistor, which is controlled by the NAND CAM cell and turned on only if there is a match in the first CAM bit. The remaining are NOR cells[3].
Drawback:

- To maintain the speed the first bit to be matched requires higher power than other bits.

3.1.2 Pipelining Scheme
The match bus is divided into many segments. The multiple match bus segments are pipelined. If there is any miss match in anyone of the stages, the other stages will be shut off, resulting in power saving.

Drawback:

- Increased latency and area overhead due to the pipeline stages.

3.1.2 Current-Race scheme
In this method the match bus is precharged low. The scheme concurrently charges the search bus to their search data values, eliminating the need for a separate SL precharge phase. After the SL/ML precharge phase completes, the enable signal, connects the current source to the match bus. A match bus in the match state charges to a high voltage, while a match bus in the miss state charges to a voltage less than that of the miss state. The maximum voltage of a miss is set to be small[3].

3.1.3 Bank-selection:
In this scheme, each search data has bank-select bit. The bank-select bit is two bit long and the CAM is divided into four blocks to store the data. The bank select bit will activate anyone of the blocks. The power consumption will be proportional to the number of the blocks [6].
Drawback:

- Due to more input combination in CAM, overflow of the banks occur. An additional circuitry is necessary to avoid overflow by re-partitioning the banks.

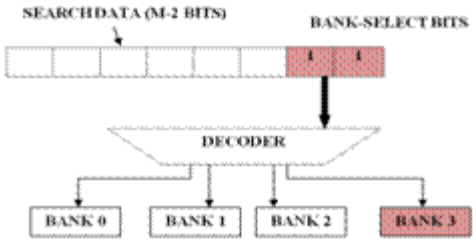


Fig.4. Bank selection based CAM Cell

3.1.4 CAM with ECC
The main idea behind the proposed scheme is to embed the ECC bits into the address of each key [8]. This procedure removes the need to store the ECC bits in a separate memory and clearly reduces the cost. Let us assume that there are such M blocks and that they correspond to the highest binary values of the n-u bits. The following procedure can be used to add a key into the CAM:

1. Compute the u ECC bits for the key.
2. Then, the positions whose *m* lower bits match those bits are checked to find one that is not occupied.
3. If such position exists, the new key is written in that address.
4. One exception is made for the positions whose upper n-u bits take a value larger than $2^{n-u} - M$. Those are not used even if they are free.

5. If no position was found in step 2, then the new key is written in any unoccupied position whose upper n – u bits have a value larger than 2n−u − M.

Drawbacks

- One potential issue of the proposed scheme is that it may not be possible to add new keys even when there are free addresses in the CAM due to the restrictions introduced.
- Sensitive to process and supply voltage variations.
- Pre computation CAM consumes more power compared to parity based CAM.
- Consumes 0.18 watt power for single search.

3.2 Proposed CAM objectives

- To reduce the search bus power, by introducing parity bits [5] as a parameter for comparison operation.
- CSC (Current Saving Control) block is added to each match bus, to reduce the match voltage to a minimum value.
- Enable signal is used to activate the CAM cells for comparison with the stored word.
- To reduce the overall power consumption of the CAM.

3.2.1 Advantages

- CAM cells are in operation only during the activation of the enable signal, due to which the unnecessary power supply for the CAM is reduced.
- The CSC block reduces the match case voltage and also the power for the MLSA is reduced.
- The parity bit reduces the memory space required, when compared with the storage of number of count of 1's in conventional CAM.
- These features make it applicable for high speed routing applications.

3.2.2 Applications

- In my paper, proposed CAM is used to replace the ATM switch in ATM networks. The drawback of ATM switches that occur during congestion is eliminated by using the proposed CAM. The queuing problem that arise in ATM switches is reduced and the cell loss is reduced by 24% by using the proposed CAM.
- CAMs are used in Network address translation and Pattern recognition.
- Content Addressable Memories are attractive for high-speed lookup-intensive applications such as packet forwarding and classification in network routers.

3.2.3 Flow diagram

The word to be searched will be placed in the data register. By using the parameter extractor the parity bit value of the word to be searched is obtained and a match is found by comparing this value with the stored word parity bit. The parity bit matched words are compared with all bits in the search word. Once a match is found, the address of the port number through which the word has to be forwarded is obtained. If a mismatch occurs then the word will be stored in the CAM cell and a port will be assigned to forward the word.

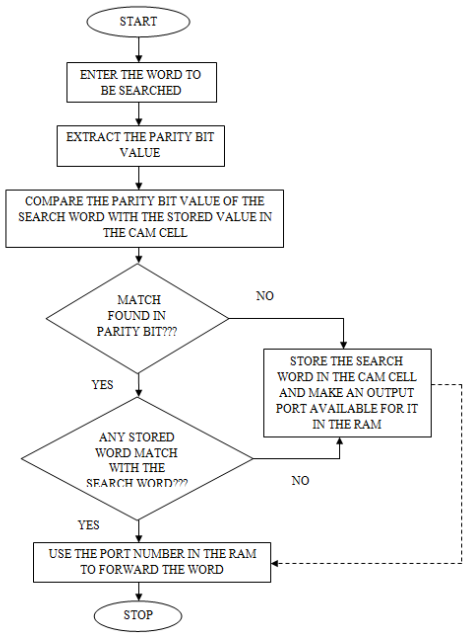


Fig.5. Flow diagram of proposed CAM cell

3.2.4 Block diagram

The data register consists of the word to be searched. The parameter extractor is used to obtain the parity bit for the search bit. The word will be broadcasted onto the search line. Only the words whose parity bit value is matched will be compared with the search word. The CAM cell consists of the stored bit in it.

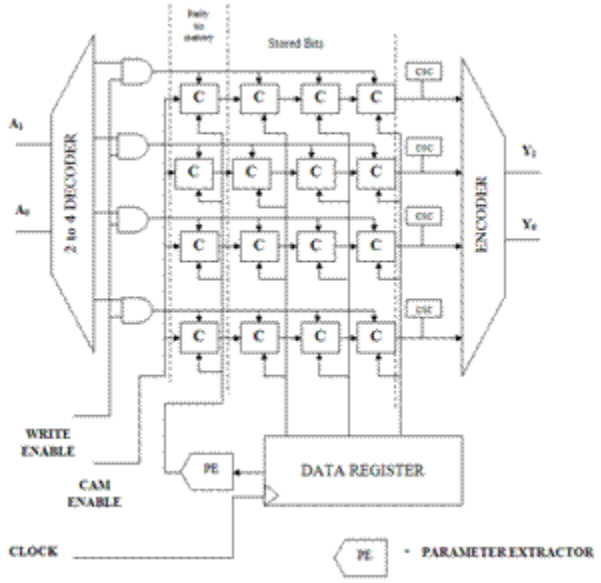


Fig.6. Block diagram of proposed CAM cell

Once the search word match with the search word the address of the match bus will be obtained at the output of the encoder. The address will be useful to forward the packets through the concern port number. The csc block in each match bus is used to reduce the power consumption of each match buss by which the overall power consumption is reduced. Additionally, an enable signal is included to enable the CAM cell for operation. The 2:4 decoder is used for the initial write operation in CAM cell. The write enable signal is used for this purpose. The parameter extractor which is the basic parity bit generator circuit is used to find the parity bit value of every search word.
3.2.5 Output

The TANNER simulator W-EDIT output is shown below. The encoder output denotes the match bus address. By using the match bus address and SRAM content the data is forwarded into the network to reach its destination. The power analysis output of T-EDIT window is shown, in which the average power consumption is 0.009 watts is obtained.

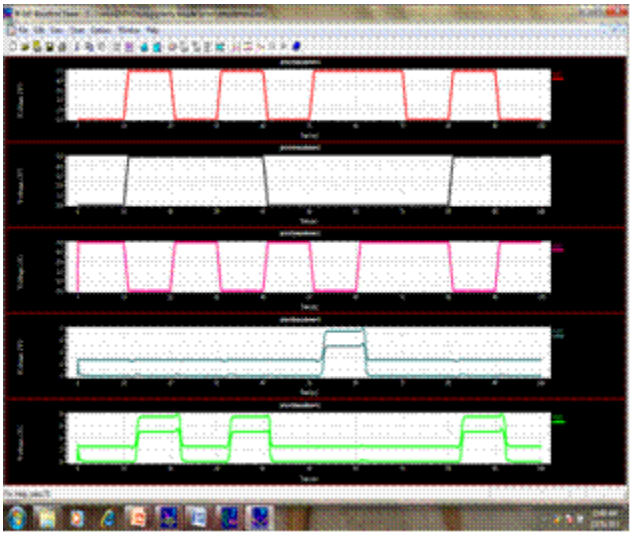


Fig.7. Tanner W-Edit output of proposed CAM

Power Analysis of proposed CAM

* BEGIN NON-GRAPHICAL DATA
- Power Results
- Average power consumed -> 0.09e-001 watts
- Max power 0.18e-001 at time 1.27025e-008
- Min power 0.000000e+000 at time 0

* END NON-GRAPHICAL DATA

4 CONCLUSION

Thus the CAM with parity bit and CSC reduces the power consumption 50% when compared with the conventional CAM. Here, schemes are introduced to reduce the power consumption of both the search buss and match buss. The chip area required to implement this scheme will be large when compared with the conventional CAMs. Error correction schemes will be added to enhance the performance of the CAMs. IN future techniques to reduce the coupling effect of adjacent match bus will be introduced to improve the performance of CAM.

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